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VHDL Modeling for Digital Design Synthesis

Yu-Chin Hsu, Kevin F. Tsai, Jessie T. Liu, Eric S. Lin

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The purpose of this book is to introduce VHSIC Hardware Description Lan guage (VHDL) and its use for synthesis. VHDL is a hardware description language which provides a means of specifying a digital system over different levels of abstraction. It supports behavior specification during the early stages of a design process and structural specification during the later implementation stages. VHDL was originally introduced as a hardware description language that per mitted the simulation of digital designs. It is now increasingly used for design specifications that are given as the input to synthesis tools which translate the specifications into netlists from which the physical systems can be built. One problem with this use of VHDL is that not all of its constructs are useful in synthesis. The specification of delay in signal assignments does not have a clear meaning in synthesis, where delays have already been determined by the im plementationtechnolo~y. VHDL has data-structures such as files and pointers, useful for simulation purposes but not for actual synthesis. As a result synthe sis tools accept only subsets of VHDL. This book tries to cover the synthesis aspect of VHDL, while keeping the simulation-specifics to a minimum. This book is suitable for working professionals as well as for graduate or under graduate study. Readers can view this book as a way to get acquainted with VHDL and how it can be used in modeling of digital designs.

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